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Electrodeposited Light-Emitting Nanojunctions

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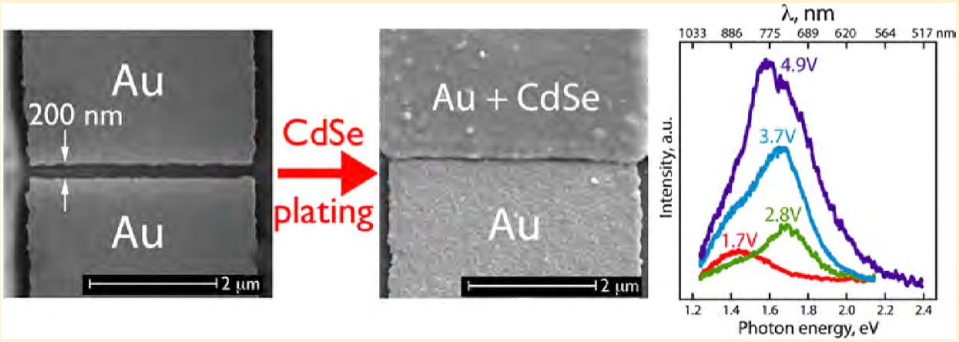

ABSTRACT: Electroluminescent (EL) metal-semiconductor-metal nanojunctions are prepared by electrodepositing nanocrystalline cadmium selenide (*nc*-CdSe) within ~250 nm gold (Au) nanogaps prepared by focused ion beam milling. The electrodeposition of *nc*-CdSe is carried out at two temperatures: 20 °C ("cold") and 75 °C ("hot"), producing mean grain diameters of 6 ± 1 nm and 11 ± 2 nm, respectively, for the *nc*-CdSe. Light-emitting nanojunctions (LEnJs) prepared at both temperatures show a low threshold voltage for light emission of <2 V; just above the 1.74 eV bandgap of CdSe. The EL intensity increases with the injection current and hot-deposited LEnJs produced a maximum EL intensity that is an order of magnitude higher than the cold-deposited LEnJs. Emitted photons are bimodal in energy with emission near the band gap of CdSe, and also at energies 200 meV below it; consistent with a mechanism of light emission involving the radiative recombination of injected holes with electrons at both band-edge and defect states. The quantum yield for "hot" electrodeposited *nc*-CdSe LEnJs is comparable to devices constructed from single crystalline nanowires of CdSe, and the threshold voltage of 1.9 (±0.1) V (cold) and 1.5 (±0.2) V (hot) is at the low end of the range reported for CdSe nanowire based devices.

KEYWORDS: *light emitting diodes (LEDs), metal−semiconductor−metal (M−S−M) junction, focused ion beam (FIB) milling, cadmium selenide, electrodeposition, polycrystalline*

INTRODUCTION

The fabrication of efficient electrically powered nanometer-scale light emitters is of interest from both a scientific and a technological standpoint.[1−4] Semiconducting nanowires have been used as the emissive elements in many previous studies, and among the architectures that have been explored are single nanowires,[5] crossed nanowires,[1,6] single nanowire superlattices,[2,7] and core/multishell nanowire heterostructures.[8] These elegant devices have been achieved using electron beam lithography (EBL) to pattern electrical contacts onto a single nanowires or nanorods, a slow, serial process.[1−8]

An alternative approach is to synthesize a semiconductor between prefabricated metal electrodes to produce metal-semiconductor-metal (or M−S−M) light-emitting junctions thereby circumventing the slow serial fabrication of electrical contacts by EBL. Metal nanogap structures have recently been used for this purpose.[9−14] The history of nanogap emissive devices begins in 2002 when Dickson and co-workers[9−11] reported electroluminescence (EL) from silver and gold nano clusters located within metal nanogaps. Park et al.[12] showed in 2005 that EL from single CdSe nanocrystals located within a metal nanogap could be detected. Mäkinen et al.[13] demonstrated in 2007 that light emission from CdSe/ZnS (core/shell) nanocrystals, tethered onto a gold surface, could be stimulated using a metal scanning tunneling microscope (STM) tip. In that case, the surface of the metal STM tip forms one end of the nanogap and a metal surface the other. Light emission from CdSe nanowires using a STM was also probed recently.[15] EL from CdSe/ZnS (core/shell) nanocrystals assembled into an asymmetric In:Pt nanogap was reported in 2008 by Bawendi et al.[14] The assembly process in that case involved solution casting of the nanocrystals onto an electromigrated platinum nanogap. A survey of prior work (Table 1) reveals that the quantum efficiency, η, for light emission from M−S−M structures including nanogaps,[5,12,14,16] $\eta = 10^{-5}$−10^{-6}, is lower and the threshold voltage for light emission, V_{th}, is higher (V_{th} = 5−15 V) than for devices based upon p-n junctions where $\eta = 10^{-2}$−10^{-5} and V_{th} = 1.7−4 V.[1,2,8,17]

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Table 1. Performance of Nanoscale Light Sources Based upon Semiconductors

emissive material[a]	E_{th}[b] (V)	quantum efficiency[c]	device type[d]	ref
CdSe NCs-PPV	4	10^{-5}–10^{-4}	P–N	17
CdSe NW	5	$(1–5) \times 10^{-6}$	M–S–M	5
CdSe NR	1.7	10^{-5}	M–S–M	12
CdSe/ZnS core/shell NCs in NG	11	N/A	M–S–M	14
CdSe/ZnS core/shell NCs in NG	15	N/A	Si–S–Si	16,45
CdS NW	2.6	10^{-3}–10^{-2}	(p-Si)–N	6
GaN NW	3.5	10^{-3}	(p-Si)–N	6
GaN CMS NW	N/A	5×10^{-2}	P–N	8
InP crossed NW	1.7	10^{-5}	P–N	1
InP superlattice NW	N/A	10^{-3}	P–N	2
***nc*-CdSe in NG**				
T_{dep} = **20°C**	**1.9(± 0.1)**	**1.2(± 0.4) × 10^{-6}**	**M–S–M**	**this work**
T_{dep} = **75°C**	**1.5(± 0.2)**	**1.8(± 0.7) × 10^{-6}**	**M–S–M**	**this work**

[a]Abbreviations: NW = nanowire; NR = nanorod; NC = nanocrystal; PPV = poly(*p*-phenylene vinylene), CMS = core multishell; NG = nanogap. [b]E_{th}, the threshold voltage for light emission. [c]The quantum yield for photon emission. [d]Abbreviations: P–N = p-n junction, M–S–M = metal-semiconductor-metal junction, Si–S–Si = silicon-semiconductor-silicon junction.

All of the examples cited above have involved an emissive element composed of a single crystalline nanoparticle or nanowire, or an ensemble of single crystalline nanostructures. Electrodeposition has not been investigated as a means for selectively functionalizing metal nanogaps with emissive semiconducting materials to our knowledge. Here we demonstrate a simple, high-throughput method for preparing nanoscale M–S–M LEnJs that exploits the electrodeposition of nanocrystalline CdSe (*nc*-CdSe) into gold nanogap structures. These nanogaps are produced by focused ion beam (FIB) milling[18] which produces uniform and reproducible nanogaps having widths of 200–250 nm in evaporated gold films. Cadmium selenide was selected as the emissive material both because stoichiometric *nc*-CdSe can be electrodeposited[19–23] and because it has a direct bandgap at 1.74 eV.[24] Previously, we have electrodeposited *nc*-CdSe to produce photoconductive nanogaps,[25] nanowire arrays for photodetectors,[22,26,27] and field-effect transistors.[28] In that work, we found that *nc*-CdSe electroplated at room temperature (T_{dep} = 20 °C) had a average grain diameter of ≈5 nm, a high electrical resistivity, and a short minority carrier lifetime which we attribute to an abundance of defect and surface states in this material.[22,25–27] Electrodepositing the *nc*-CdSe from hot solution (T_{dep} = 75 °C) increases the grain diameter by a factor of two, enhancing the carrier mobility and the electronic conductivity of the material.[25,27] In this paper, we examine the properties of LEnJs prepared using *nc*-CdSe deposited both at 20 and 75 °C. The properties of *nc*-CdSe are ideal for the fabrication of fast photodetectors, but the high defect density of these materials are not optimal for making efficient light-emitting devices. Nevertheless, the LEnJs described here are characterized by a quantum efficiency for EL, η, ranging from $1.2(\pm0.4) \times 10^{-6}$ (cold) to $1.8(\pm0.7) \times 10^{-6}$ (hot), values that approach the η for single crystalline CdSe nanowires ($\eta = 10^{-5}$–10^{-6}) in symmetrical M–S–M devices (Table 1).[5,12] In addition, we observe a voltage threshold for light emission, V_{th}, of 1.9(±0.1) V (cold) and 1.5(±0.2) V (hot) that is at the low end of the range reported for CdSe nanowire based devices ($V_{th} \approx 1.7$–5 V)[5,12]

EXPERIMENTAL SECTION

Chemicals and Materials. Cadmium sulfate ($CdSO_4 \cdot 8H_2O$, 98+%), selenium oxide (SeO_2, 99.9+%), iodine (I_2, 99.8+%), and chromium etchant were used as received from Sigma-Aldrich. Sulfuric acid (ULTREX ultrapure) was purchased from J. T. Baker. Potassium iodide (KI, 99%) and acetone were used as received from Fisher (ACS Certified). Positive photoresist (Shipley, S1808) and developer (Shipley, MF-319) were purchased from Microchem Corporation. Gold pellets (5N purity, ESPI Metals) and chromium powder (3N purity, American Elements) were used for the evaporation of films.

Device Fabrication. As illustrated in Figure 1a, the process started from thermally evaporating a Cr/Au (1/40 nm) thin film onto precleaned 2.5 × 2.5 cm squares of soda lime glass. Cr was used here as an adhesion layer. A positive photoresist (PR) layer (Shipley, S1808) was spin coated (2500 rpm, 80 s), and a PR layer of ∼800 nm thickness was formed after soft-baking (90 °C, 30 min). The PR was then patterned using a quartz contact mask in conjunction with a UV light source (365 nm, 500 W, × 2 s) equipped with a photolithographic alignment fixture (Newport, 83210-V). Either of two different masks were employed in this work, the first had gold finger widths of 5 μm spaced by 5 μm, and the second had 20 μm gold fingers spaced by 20 μm. Identical results were obtained with these two masks. The exposed PR region was developed for 25 s (Shipley, MF-319) and rinsed with Millipore water (Milli-Q, ρ> 18 MΩ·cm). Exposed Au and Cr was removed by dipping in $KI/I_2/H_2O$ (4/2/40 g) solution for 10 s and standard Cr etchant (Aldrich) for 3 s, respectively, resulting in six independent 12-finger patterns. Etching reduced the total width of gold fingers by approximately 1 μm, as seen for example in Figure 3 where the finger width is 4 μm instead of 5 μm. The PR layer was then removed with acetone, and FIB milling was used to create 200–250 nm nanogaps across these gold fingers. FIB milling was accomplished using a FEI Quanta 3D DualBeam (FIB/SEM) system, equipped with a Ga liquid metal ion source operating at 30 keV and 10 or 30 pA.

Electrodeposition of *nc*-CdSe. *nc*-CdSe was electrodeposited into these nanogaps by potentiostatic deposition at −0.6 V vs SCE, from solutions maintained at 20 °C or heated to 75 °C using a hot plate. The plating solution was unstirred aqueous 0.30 M $CdSO_4$, 0.70 mM SeO_2, and 0.25 M H_2SO_4 at pH 1–2. (***Caution!*** *Both $CdSO_4$ and SeO_2 are highly toxic.*) Electrodeposition was conducted in a one-compartment three-electrode electrochemical cell using a saturated calomel reference electrode (SCE) and a platinum counter electrode in conjunction with a Gamry G300 potentiostat. Films prepared at 20 °C were deposited for 500 s while those prepared at 75 °C were deposited for 100 s. These deposition times yielded *nc*-CdSe films that were 300–400 nm in thickness on the source side of the junction. After CdSe electrodeposition, the sample was rinsed with Millipore water and air-dried. No postelectrodeposition thermal treatment was carried out.

Structural Characterization. Scanning electron microscopy (SEM) images were acquired using FEI Quanta 3D or FEI Magellan systems. Before CdSe electrodeposition, the nanogaps were examined

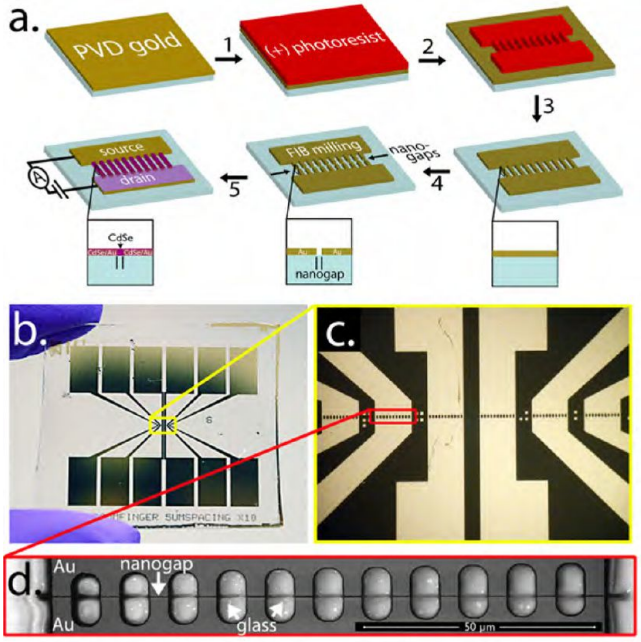

Figure 1. Fabrication of a Au-CdSe-Au nanogap LEnJs. (a) Schematic process flow for creating a nanogap and electrodeposition of *nc*-CdSe into it: (0) A 1 nm/40 nm Cr/Au thin film is thermally evaporated onto a glass substrate, (1) a (+)-photoresist (PR) layer is spin-coated onto the gold film, (2) the PR layer is photo patterned using a quartz contact mask in conjunction with a 365 nm mercury lamp, (3) after development, exposed Au is etched away together with PR residue, (4) FIB milling is used to cut 200−250 nm wide nanogaps in these bridges, (5) electrodepositing *nc*-CdSe into the nanogap. (b) Photograph of a 2.5 × 2.5 cm glass slide with six independent twelve-bridge structures in the center. (c) Optical micrograph of the six twelve-bridge structures. (d) Scanning electron micrograph of a twelve junction device with 5 μm gold fingers after the fabrication by FIB of 200−250 nm nanogaps. Twelve junction arrays were also prepared using a second mask that defined 20 μm gold fingers spaced by 20 μm for use in some measurements.

at an accelerating voltage of 5 keV without metal coating. After deposition, the sample was reexamined at 10 keV after plasma coating with Au/Pd to ameliorate charging. EDX spectra were collected on an FEI Quanta 3D equipped with a 50 mm^2 silicon drift X-ray detector (Oxford instruments, X-MAX).

Grazing-incidence X-ray diffraction (GIXRD) patterns were obtained using a Rigaku Smartlab X-ray diffractometer employing the parallel beam optics (PB/PSA) with a fixed incident angle of 0.3°. The X-ray generator was operated at 40 kV and 44 mA with Cu K_α irradiation. The integrated Rigaku PDXL X-ray pattern data processing software was used to analyze acquired patterns and estimate the mean grain diameter.

Transmission electron microscopy (TEM) images and selective area electron diffraction (SAED) patterns were obtained using a Philips CM-20 TEM operating at 200 keV. An SAED aperture of 2.5 μm was used, and the diameter of the selected specimen area was ∼100 nm. Samples for TEM analysis were prepared by patterning the *nc*-CdSe-filled gold nanogap on top of a 10 nm thick Si_3N_4 membrane window centered on a 200 μm thick silicon frame (Norcada Inc.).

Characterization of EL Emission. EL measurements were carried out at room temperature in laboratory air using an inverted optical microscope outfitted with a CMOS camera and a spectrograph with a CCD detector (Figure 2). In more detail, an inverted microscope (Olympus, IX71) equipped with a 40× objective lens (Olympus, LUCPlanFLN 40 × /0.60) was used to acquire EL images as a function of bias using a CMOS camera (Andor, Neo); EL emission spectra were obtained with the same microscope and objective using a

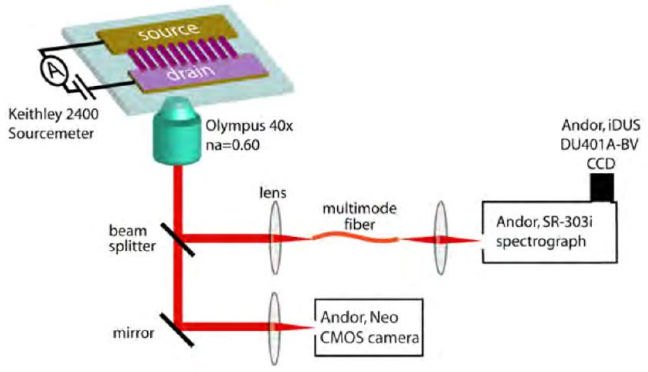

Figure 2. Schematic of the apparatus used to acquire EL images and emission spectra.

spectrometer (Andor, Shamrock SR-303i) equipped with a 300 l/mm grating blazed at 500 nm. EL spectra were detected using a CCD camera (Andor, iDUS DU401A-BV). Electrical measurements were accomplished using a sourcemeter (Keithley Instruments 2400), and these data were recorded using a computer controlled with LabVIEW (National Instruments) program.

RESULTS AND DISCUSSION

Fabrication of Light-Emitting Nanojunctions (LEnJs). Our process (Figure 1a) begins with the fabrication of a 40 nm thick gold film that is patterned to produce six sets of twelve 5 μm-wide fingers using a combination of thermal evaporation (step 0), photolithography (step 1 and 2), and chemical etching (step 3). Nanogaps are then produced across each finger by FIB milling (step 4). Finally, a *nc*-CdSe film is electrodeposited, initially on one-half of the nanogap structure. With continued deposition, the *nc*-CdSe film bridges across the nanogap to complete the LEnJ (step 5). Six nanogap arrays, each with twelve 5 μm-wide nanogaps, were patterned onto 2.5 × 2.5 cm glass slides (Figure 1b). An optical micrograph (Figure 1c) shows the device before the electrodeposition of *nc*-CdSe. One of the six independent nanogap arrays was reserved for characterization by scanning electron microscope (SEM) (Figure 1d). Each nanogap, prepared by FIB milling, was 200−250 nm in width (Figure 3a,c). The electrodeposition of *nc*-CdSe onto one side of this junction bridges across this gap, completing the electrical circuit (Figure 3b,d).

In principle, the process depicted in Figure 1a is scalable and could be used in conjunction with photolithography and automated FIB milling to produce LEnJs on the wafer scale. The electrodeposition of stoichiometric, crystalline, *nc*-CdSe is the most critical component of this process. Previously, we have electrodeposited near-stoichiometric *nc*-CdSe using the scanning electrodeposition/stripping method[19,22,26,27] but in the present case we found that scanning the potential of the nanogap caused it to erode, increasing its width.[25] Miller et al.[29] used similar plating solutions to prepare CdSe films for photoelectrochemistry applications using potentiostatic deposition at −0.60 V vs SCE. In that work, however, X-ray diffraction and elemental analysis data for these films were not reported. Based upon this precedent, we electrodeposited *nc*-CdSe by potentiostatic electrodeposition using the same solution as we have used previously: 0.3 M $CdSO_4$, 0.7 mM SeO_2, and 0.25 M H_2SO_4, pH 1−2.[19,26,27] As the potential of a gold electrode is scanned negatively from −0.30 V to −0.70 V in this solution, (Figure 4a, blue trace) a gradual increase in

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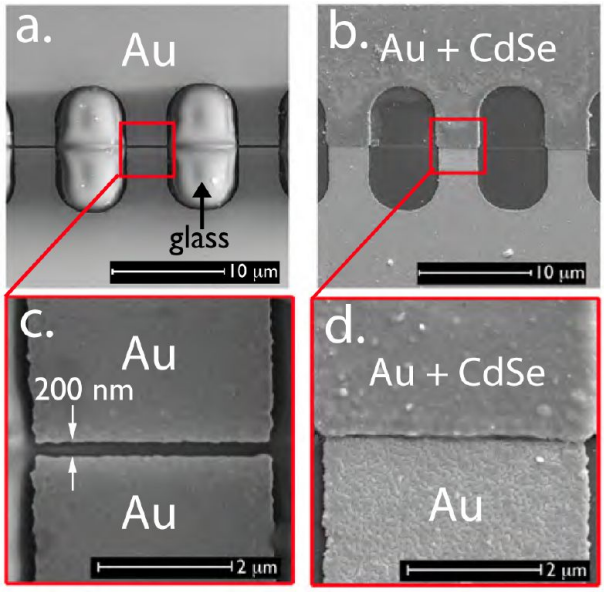

Figure 3. SEM characterization of a nascent LEnJ before and after electrodeposition of *nc*-CdSe. (a,b) Scanning electron micrographs of nanogaps formed by a single FIB milling (a) and same nanogaps after the electrodeposition of *nc*-CdSe (b). (c,d) Zoomed in micrographs of the nanogap before (c) and after (d) the electrodeposition. The white background in (a) is caused by charging since the surface was not subjected to metal coating prior to SEM imaging. *nc*-CdSe initially grows only on the top gold electrode, on one side of the nanogap, because only this electrode was connected to the potentiostat.

cathodic current is observed (Figure 4a, process (i)). Three reactions occur in this potential range[29,30]

$$H_2SeO_3 + 4H^+ + 4e^- \rightarrow Se(s) + 3H_2O \quad (1)$$

$$Cd^{2+} + Se(s) + 2e^- \rightarrow CdSe(s) \quad (2)$$

$$Cd^{2+} + H_2SeO_3 + 4H^+ + 6e^- \rightarrow CdSe(s) + 3H_2O \quad (3)$$

Reactions 1 and 2, both of which have H_2SeO_3 directly or indirectly as a reactant, are reduced in importance relative to process 3 as the concentration of H_2SeO_3 is reduced relative to that of Cd^{2+}.[30,29] At potentials negative of −0.70 V to −0.75 V, cathodic current associated with cadmium metal deposition augments the current resulting from reactions 1−3 (Figure 1a, process (ii))

$$Cd^{2+} + 2e^- \rightarrow Cd(s) \quad (4)$$

On the subsequent positive-going scan, metallic cadmium is anodically stripped from the nascent CdSe deposit at ∼−0.45 V (Figure 1a, process (iii))

$$Cd(s) \rightarrow Cd^{2+} + 2e^- \quad (5)$$

We found that stoichiometric, cubic *nc*-CdSe was obtained by potentiostatic deposition at any potential in the range from −0.40 V to −0.61 V. Heating the plating solution to 75 °C increases the cathodic deposition current over this entire potential range (Figure 4a, red trace), accelerating the rate of CdSe deposition at −0.60 V by a factor of 5.

To fill an array of gold nanogaps with electrodeposited *nc*-CdSe, one side of the nanogap array was designated as a working electrode, and it was electrically connected to the potentiostat. The nanogap was then immersed into the plating solution, and the potential was stepped from the open circuit value to −0.60 V. At this potential, a time-invariant steady-state deposition current was observed within a few seconds (Figure 4b). After 300 s (T_{dep} = 20 °C) or 50 s (75 °C), the current rapidly increased as the nanogap filled with *nc*-CdSe, bridged to the other gold contact, and the electrodeposition of *nc*-CdSe commenced on the initially clean side of the gold nanogap as shown schematically in the inset of Figure 4b (inset). These "bridging times" were reproducible (±5%) from device to device in this study. *nc*-CdSe deposition was terminated at deposition times that were greater than these bridging times: 500 s (20°C) or 100 s (75°C). At these longer times, the deposition current has already stabilized at the new, higher steady-state value: a signature that all twelve nanogaps in the array were filled. These deposition times were selected empirically because they produced identical *nc*-CdSe layer thicknesses of 300−400 nm in the nanogap at both temperatures: 20°C and 75°C. Optical micrographs of a device (Fig 4c−e) show the gold electrode before deposition (c), during the initial, steady-state deposition of *nc*-CdSe onto one side of the nano gaps (d), and after the nanogap is bridged and *nc*-CdSe has been deposited on both sides of the nanogap (e). The variation in the color of the *nc*-CdSe across the device is caused by small variations in the *nc*-CdSe thickness.

Cadmium Selenide Characterization. Grazing incidence X-ray diffraction patterns (GIXRD, Figure 4f) show reflections that are assignable to cubic CdSe (JCPDS 88-2346) and no reflections corresponding to either elemental cadmium or selenium. The narrower line widths seen in the pattern for *nc*-CdSe deposited at 75 °C is a consequence of the larger mean grain diameter for that sample as compared to *nc*-CdSe prepared at 20 °C. Scherrer analyses[31] of the (111) or (220) reflections yields a mean grain diameter of 11 ± 2 nm and 6 ± 1 nm for the 75 °C sample and the 20 °C, respectively. A shoulder on the low angle side of the (111) reflection, seen in both of the GIXRD patterns, shows that some hexagonal phase is present in these predominantly cubic films (Figure 4f). Energy-dispersive X-ray spectroscopy (EDX) patterns show that the *nc*-CdSe films prepared at both temperatures are approximately stoichiometric (Figure 4g).

nc-CdSe films were also investigated using TEM and SAED (Figure 5). SAED patterns for *nc*-CdSe prepared at 20 °C consist of diffuse, continuous diffraction rings centered at *d*-spacings that index to cubic CdSe (JCPDS 88-2346, Figure 5a). Since the sample diameter in this measurement was ∼100 nm (using a 2.5 μm aperture), it is apparent that these continuous rings are derived from grains that are much smaller than this. In contrast, discontinuous rings are seen at the same *d*-spacings in the SAED patterns for the samples prepared at 75 °C, indicating that a smaller number of grains are contributing to diffraction for this sample which was also ∼100 nm in diameter. We conclude that the grain diameter for the films prepared at 75 °C is larger than for films prepared at the lower temperature. Lattice-resolved TEM images (Figure 5c,d) also reveal the polycrystalline nature of the *nc*-CdSe deposited at both temperatures. At higher magnification (Figure 5e,f), lattice fringes spaced by 0.35 nm are observed, corresponding to the *d*-spacing along the [111] lattice direction of cubic CdSe.

Light Emission from Nanogaps. Optical micrographs of LEnJ arrays were recorded as a function of the applied voltage bias (E_{app}, Figure 6a,b). These images show that the intensity of light emission from LEnJs and the number of emissive

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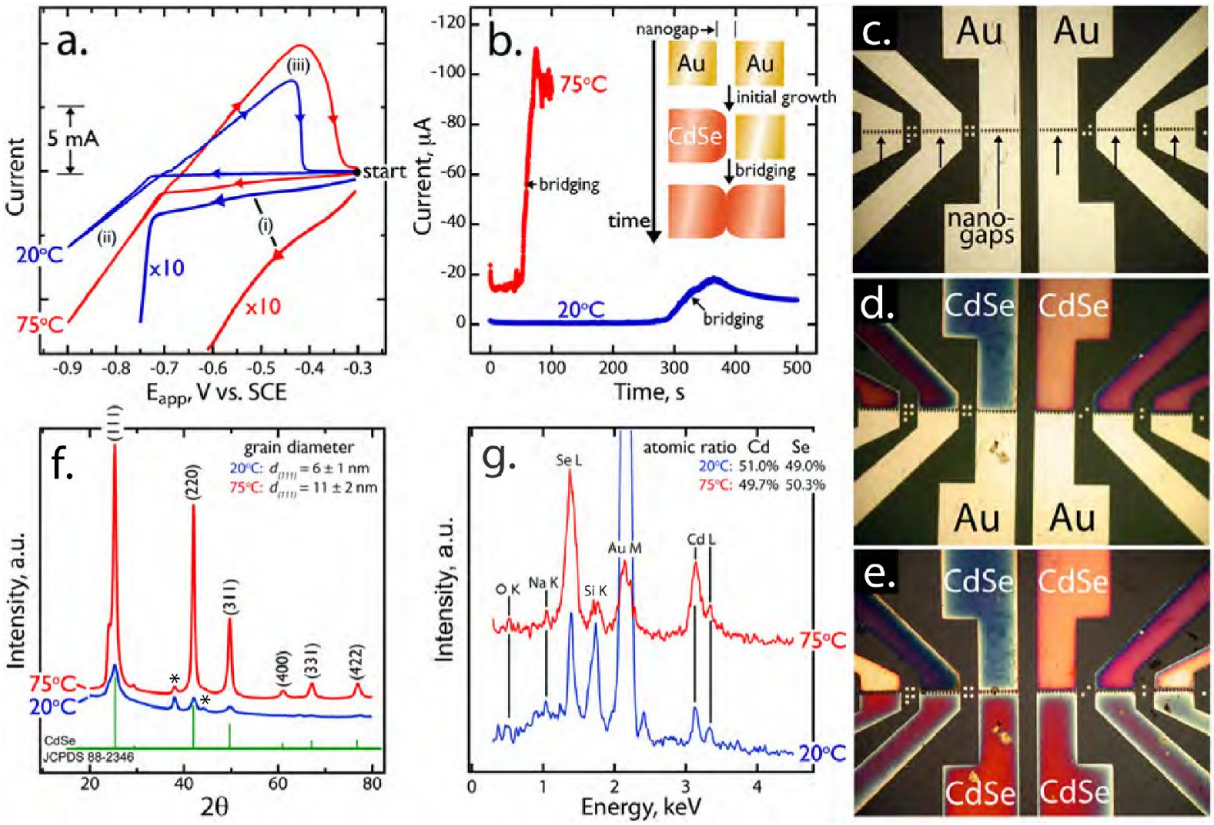

Figure 4. Electrodeposition and characterization of *nc*-CdSe electrodeposited at 20 °C (blue) and 75 °C (red). (a) Cyclic voltammetry (50 mV/s) of a plating solution containing Cd^{2+} (0.3 M), SeO_3^{2-} (0.70 mM), pH = 1−2, adjusted with H_2SO_4. Peak (i) is scaled by a factor of 10 for clarity. Peak (i) is assigned to reactions 1, 2, and 3 in the text; peak (ii) is assigned to reaction 4; peak (iii) is assigned to reaction 5. (b) Current versus deposition time for the electrodeposition of *nc*-CdSe at a potential of −0.6 V vs SCE. Inset shows the schematic growth diagram. (c−d) Optical micrographs of a patterned gold electrode before deposition of *nc*-CdSe (c), after the deposition of *nc*-CdSe on one side of the nanogap (d), and after deposition has occurred on both sides of the nanogap (e). (f) Grazing incidence X-ray diffraction (GIXRD) pattern acquired for a *nc*-CdSe thin film electrodeposited on a Au film on glass. Prominent reflections are assigned to cubic CdSe (JCPDS 88-2346). At 75 °C, the bigger grain size yields sharper peaks. Peaks marked with an asterisk (*) are contributed by the gold electrode. (g) Energy-dispersive X-ray (EDX) analysis of *nc*-CdSe prepared at 20 °C (blue) and 75 °C (red) showing that both materials are approximately stoichiometric.

junctions, both increase with E_{app}. Pronounced differences are seen between the array prepared at T_{dep} = 20 and 75 °C: at E_{app} = 2.8 V, a minority of the LEnJs prepared at T_{dep} = 20 °C are emissive while all of the junctions prepared at T_{dep} = 75 °C emit light. Moreover, a lower threshold voltage for light emission, E_{th}, of 1.4 V is seen for 75 °C junctions whereas E_{th} is 1.9 V for LEnJs prepared at T_{dep} = 20 °C. A plot of EL intensity versus position along the array of ten nanogaps for E_{app} = 2.5 V show that the peak light intensity of each emitter in the array is an order of magnitude higher for the T_{dep} = 75 °C than for T_{dep} = 20 °C (Figure 6c,d). Individual emitting regions, characterized by a full-width at half-maximum intensity of ≈1 μm, are much smaller than the width of the nanogap and multiple emitters are seen in many of the nanogaps for the array prepared at 75 °C (Figure 6e,f). These images show that the EL efficiency of the electrodeposited *nc*-CdSe at both temperatures varies widely as a function of position even within a single filled nanogap in spite of the fact that the chemical composition probed by EDX and the morphology of these films seen by SEM appear to be uniform at the resolution of these methods.

Each LEnJ is a gold−(*nc*-CdSe)−gold M−S−M diode consisting of two, back-to-back Schottky diodes. The rectification produced by a single Schottky diode can be understood entirely with reference to the majority carriers: the Au-CdSe interface shows a low resistance to electron transfer from CdSe to gold when a negative bias is applied to the CdSe side of the junction, but a high resistance for electron flow in the opposite direction, corresponding to a negatively biased Au electrode. For the reversed biased junction, electron flow is blocked by a barrier of ϕ_n = 0.49 eV in the case of Au/CdSe.[24] In contrast, Sze et al.[32] showed 40 years ago that *both* electrons and holes contribute to the total current measured in a typical M−S−M device. The application of a voltage bias as shown in Figure 8d, drives the Au_1−CdSe interface at the negative side to be reversed biased, while the interface on the positive side CdSe-Au_2 interface is forward biased. The reverse biased interface limits the flow of electrons across the device[24,32−34] but as E_{app} is increased and the bands at the CdSe-Au_2 interface are flattened the barrier to hole injection and transport across the device is reduced by V_{bi2}, the built-in voltage (Figure 8c), and the total current increases accordingly.[32] Concurrently, both barriers ϕ_{n1}, for electrons at Au_1, and ϕ_{p2}, at Au_2, are further reduced by the Schottky effect:[24] for example, $\phi_{n1} = (q\mathcal{E}/4\pi\varepsilon_s)$ where $\mathcal{E}$ is the electric field and ε_s is the dielectric constant. Finally, the electric field-induced barrier lowering that forms the basis for the Schottky effect can also operate at shallow traps in the semiconductor, releasing additional carriers in a phenomenon called Poole−Frenkel emission.[35,36]

With this as background, what information can be extracted from current versus voltage curves? For both Au-CdSe-Au

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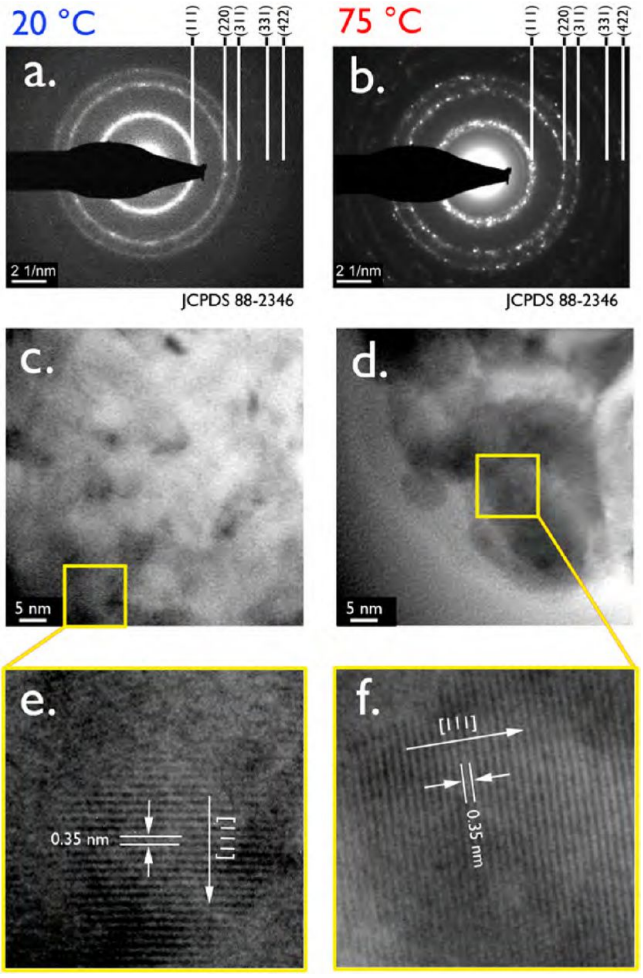

Figure 5. Selected area electron diffraction (SAED) patterns and transmission electron micrographs (TEM). (a,b) SAED patterns for *nc*-CdSe prepared at 20 °C (a) vs 75 °C (b). (c,d) Corresponding TEM images for *nc*-CdSe prepared at T_{dep} = 20 °C (c) and 75 °C (d). (e,f) Higher magnification views of individual grains showing the lattice fringes along the [111] direction.

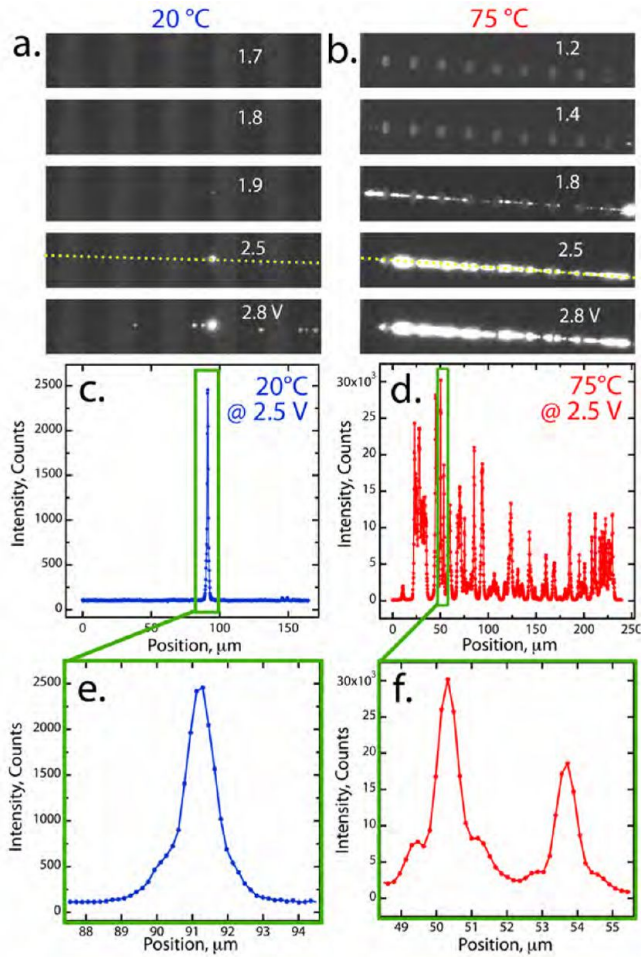

Figure 6. Optical micrographs and intensity profiles for LEnJs. (a,b) Optical micrographs showing EL as a function of the applied voltage (indicated in white). Data for T_{dep} = 20 °C (a) and 75 °C (b) are shown. All images were acquired using an integration time of 10 s. The dotted yellow line in the 2.5 V image coincides with the location of the nanogaps in these images. (c,d) Intensity profiles for 20 °C (c) vs 75 °C (d) along above dashed lines at 2.5 V. (e,f) Magnified traces of emission spots reveal that the full width at half-maximum intensity of each peak is ≤1 μm.

nanogap devices fabricated at 20 °C (blue) vs 75 °C (red), *I*−*V* curves are highly symmetrical. This indicates that the growth direction for the CdSe does not influence the electronic properties of the device: the resistance to transport is the same with both voltage polarities. The exact value of the ohmic resistance, *R*, of the *nc*-CdSe in these two devices can not be measured from the complex *I*−*V* curve of Figure 7a,b; however *R* can be approximated from d*V*/d*I* evaluated at E_{app} = 2.0 V.[34] Using this estimate, the electrical resistance of the *nc*-CdSe device prepared at 20 °C is ∼260 times higher than that prepared at 75 °C. The lower resistance of the LEnJ prepared at 75 °C could be a manifestation of the larger grain diameter in the *nc*-CdSe or a higher dopant density in these samples; however, the relative importance of these two variables can not be determined from our data. Second, the LEnJs prepared at both temperatures showed symmetrical *I*−*V* curves (Figure 7a,b) similar to those previously reported for CdSe thin (≈ 500 nm) film M−S−M devices where gold contacts were employed.[37,38] In contrast to the *I*−*V* behavior of M−S−M junctions with greater semiconductor thicknesses (>1 μm), discrete transitions corresponding to the reach-through and flat-band conditions are not observed in these data.[24,32] Instead, plots of *Ln I versus* $\sqrt{V}$ are linear for both polarities (Figure 7b, inset). As already indicated above, this functionality for current−voltage curves is predicted for conduction that is limited by Schottky emission (eq 6) or Poole−Frenkel emission (eq 7):[24,36,39]

$$I = AT^2 \exp\left(-\frac{\phi_s}{kT}\right) \exp\left(\frac{\beta_s V^{1/2}}{kTd^{1/2}}\right) \quad (6)$$

$$I = I_0 \exp\left(\frac{\beta_{pf} V^{1/2}}{kTd^{1/2}}\right) \quad (7)$$

where *A* is the Richardson constant, ϕ_s is the Schottkey barrier height, *d* is the thickness of the semiconductor layer, I_0 is the low-field current, and β_s and β_{pf} are, respectively, the Schottky and Poole−Frenkel field-lowering coefficients.[24,39] These two mechanisms can be distinguished using the temperature dependence of the *I*−*V* behavior, which was not measured here. If purely Poole−Frenkel emission is occurring, then β_{pf} =

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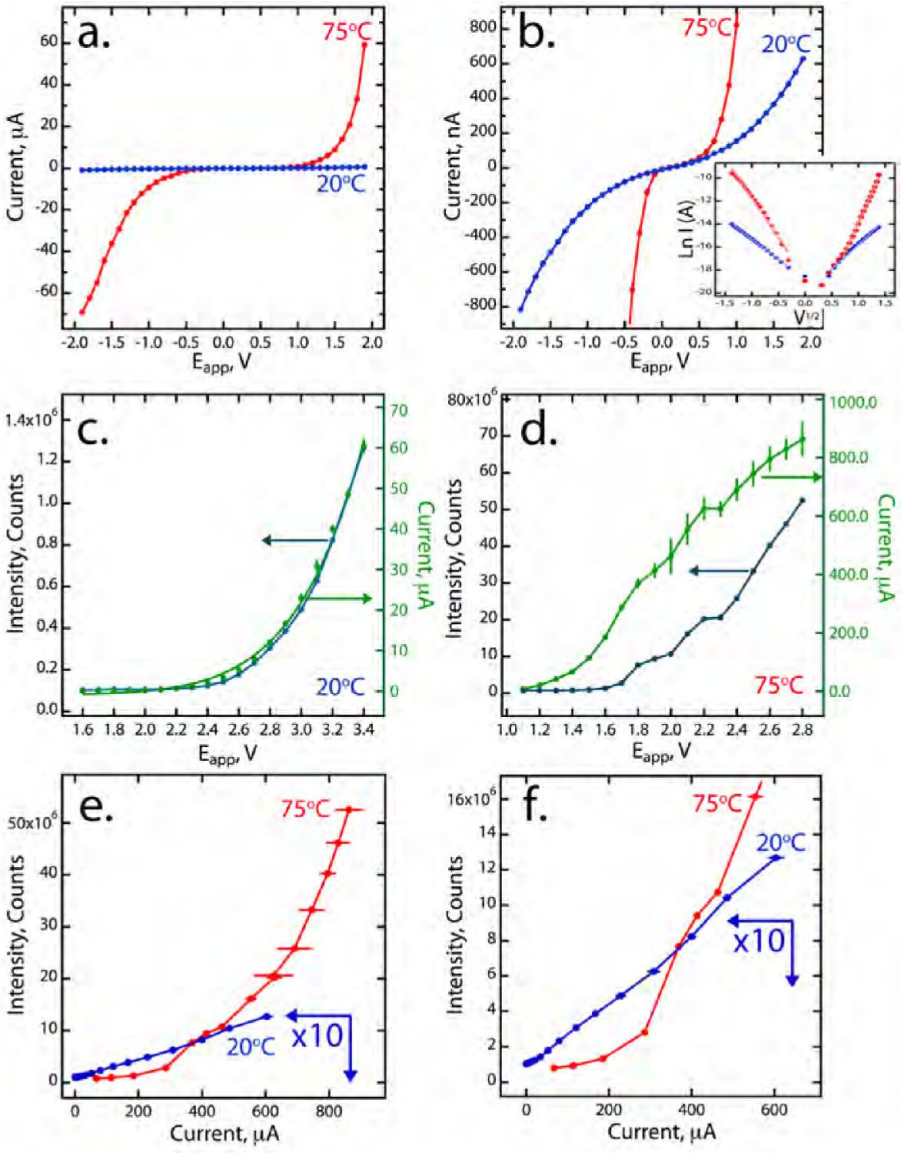

Figure 7. Electrical and optical characterization of LEnJs. (a) Current versus applied bias for Au-CdSe-Au nanogap devices fabricated at 20 °C (blue) vs 75 °C (red). (b) The same $I-V$ data shown in (a) with rescaled current axes. Inset: Plot of Ln I versus $V^{1/2}$ for these data showing the linearity of these plots. (c,d) EL intensity (left axis) and current (right axis) versus applied forward bias at 20 °C (c) vs 75 °C (d). (e) EL intensity versus current at 20 °C (blue) vs 75 °C (red), data extracted from graph (c,d). The intensity and current in blue curve are magnified by 10 times. (f) Replots of graph (e) with rescaled intensity axis. The integration time for each bias step is 10 s. Error bars show $\pm 1\sigma$ for currents measured at each applied voltage.

$(e^3)/(\pi\varepsilon_s)^{1/2}$. For $\varepsilon_s = 7.82 \times 10^{-11}$ F/m, the theoretically expected value for CdSe is $\beta_{pf} = 2.55 \times 10^{-5}$ eV $m^{-1/2}$ $V^{1/2}$ whereas we measure (Figure 6b, inset) $\beta_{pf} \approx 4.2 \times 10^{-5}$ eV $m^{-1/2}$ $V^{1/2}$ for $T_{dep} = 20$ °C and 9.0×10^{-5} eV $m^{-1/2}$ $V^{1/2}$ at $T_{dep} = 75$ °C.[39]

The intensity of the light emitted from these LEnJs is correlated with E_{app} (Figure 7c,d) and with the device current (Figure 7e,f). The lower voltage threshold seen in Figure 6 for the $T_{del} = 75$ °C device is also apparent in these data (Figure 7c,d). Since the generation of light in these devices involves the annihilation of holes and electrons (vide infra), the implication is that the injection of minority carriers (i.e., holes) into the n-type CdSe occurs at a rate that is related to the total current. The EL quantum yields (photons/electron) are calculated to be 1.2×10^{-6} ($T_{dep} = 20$ °C) and 1.8×10^{-6} ($T_{dep} = 75$ °C). These values are approximately equal to the EL quantum yield reported for single crystalline CdSe nanowire M−S−M devices.[5] However our threshold voltages, V_{th}, of 1.5−1.9 V are less than half that seen for the CdSe nanowire device in that prior work.[5]

EL spectra were obtained for $T_{dep} = 75$ °C M−S−M devices (Figure 8a,b), but the lower emission intensity for devices prepared at $T_{dep} = 20$ °C (down by a factor of 40−50) was insufficient to allow for the acquisition of spectra. The two spectra (Figure 8a,b) have the following elements in common: (1) the onset of light emission occurs at ≈ 1.2 eV which coincides with V_{th}, (2) the energy at which the EL intensity maximum is seen blue-shifts to 1.6 eV with increasing applied voltage, V_{app}, (3) The EL intensity increases monotonically with V_{app}, (4) the maximum energy of emission is in the 2.0−2.2 eV range even when $V_{app} > 4.0$ V (e.g., Figure 8a)

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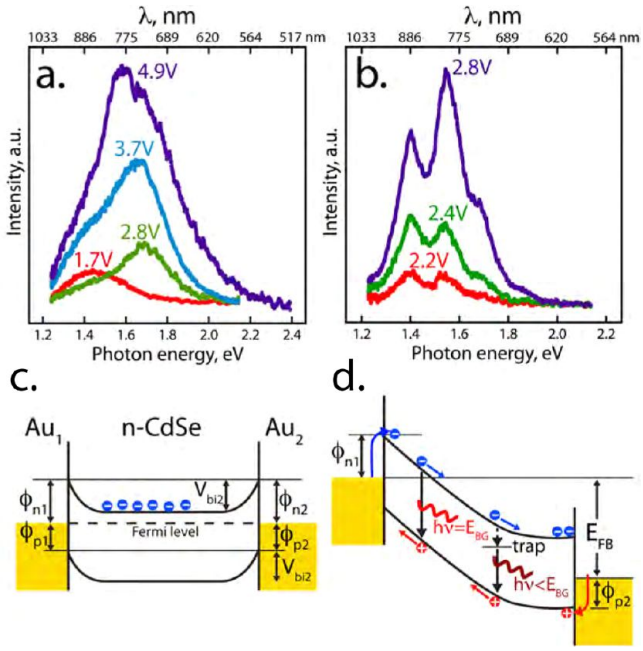

Figure 8. Electroluminescence spectra and energy level diagrams. (a,b) Examples of two EL emission spectra for LEnJs prepared from T_{dep} = 75 °C plating solutions. (c,d) Energy level diagrams depicting the M–S–M at equilibrium (c) and at an applied bias equal to the flat-band potential of the device, E_{FB} (d) showing a reduction in the barrier for hole injection by V_{bi2}. Also depicted in (d) are two radiative recombination processes for electrons and holes responsible for the EL emitted by these devices.

Mechanism of Light Emission. Several mechanisms have been proposed to account for electrically stimulated light emission from M–S–M junctions, including the resonant tunneling of electrons and holes into the *nc*-CdSe,[24,40] inelastic electron tunneling (IET)[12,41,42] and minority carrier-injection and radiative recombination.[32] Our data is fully consistent with the latter mechanism, represented by the diagram of Figure 8c,d, that is based upon the known mechanism of conduction for M–S–M junctions.[32] As shown in Figure 8d, the injection of majority carriers at Au_1 and minority carriers at Au_2 occurs concurrently and the recombination of these carriers in the CdSe is responsible for EL. Minority carrier injection significantly contributes to the total measured current as evidenced by the fact that EL emission is either directly proportional to the current (T_{dep} = 20 °C) or highly correlated with it (T_{dep} = 75 °C) (Figure 7e,f). Thus, the intensity dependence of the emission on E_{app} derives simply from increased minority carrier injection at higher E_{app}. Emission at 1.2 eV, below the band gap, is explained by the presence of traps in our *nc*-CdSe, which is highly defective. Within this picture, emission at energies above the 1.74 eV band gap of CdSe may derive from the recombination of electron and holes within nanoscopic grains having a locally larger band gap as a consequence of exciton quantum-confinement.[43,44]

CONCLUSIONS

We report the fabrication of light-emitting nanojunctions prepared by the electrodeposition of *nc*-CdSe. These are the first devices based upon electrodeposited semiconductor layers that produce measurable electroluminescence, to our knowledge. These LEnJs emit near-infrared light with a low threshold voltage of V_{th} of 1.5–1.9 V and a quantum yield of $\approx 10^{-6}$. These performance metrics are similar to those measured previously for single crystalline CdSe nanowires[5] and nanorods.[12] We compared devices prepared from *nc*-CdSe electrodeposited at room temperature with *nc*-CdSe deposited from hot plating solutions (T_{dep} = 75 °C). In the hot solution, the mean grain diameter was larger by a factor of 2, the quantum yield for light emission was larger by 50%, the threshold voltage for light emission was reduced by 40%.

The fact remains that the quantum yield for light emission is very low in this system and, based upon the literature data collected in Table 1, low QEs are endemic to devices with nanoscale emissive elements. Additional work will be required to determine the origin of low QEs and whether they can be increased significantly for electrodeposited semiconductors by adjusting the electrodeposition conditions. The feasibility of creating LEnJs using a high throughput approach, involving formation of gold nanogap array by FIB milling followed by electrodeposition of *nc*-CdSe directly in, and across, this nanogap, is demonstrated by the results presented here.

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Notes

The authors declare no competing financial interest.

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